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a substrate including a first pixel region, a second pixel region, and a third pixel region, the first pixel region and the third pixel region being disposed at both sides of the substrate with the second pixel region disposed therebetween;

a plurality of gate lines and data lines on the substrate;

- 5 a plurality of thin film transistors each formed on the first to third pixel regions, the thin film transistor including a gate electrode, a source electrode, and a drain electrode; and a pixel electrode on the substrate,

wherein overlapping widths between the drain electrode and the gate electrode vary among the first to third pixel regions.

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5. The array substrate of claim 4, wherein the overlapping width of the drain electrode is the greatest in the first pixel region, and is greater in the third pixel region than in the second pixel region.

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6. The array substrate of claim 4, further comprising a common electrode formed on the substrate and being parallel to the pixel electrode.

7. The array substrate of claim 4, wherein a distance between the source electrode and the drain electrode is constant in the first to third pixel regions.

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8. A liquid crystal display device comprising:

first and second substrates;

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a gate line and a data line on the first substrates, the gate and data lines being formed on a plurality of pixel regions;

a common line on the first substrate;

a plurality of common and pixel electrodes on the first substrate;

5 a thin film transistor having a gate electrode, a source electrode, and a drain electrode at a crossing point of the gate and data lines, wherein a capacitance between the gate electrode and the drain electrode varies in accordance with a position of the

corresponding pixel region; and

a liquid crystal layer between the first and second substrates.

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9. The device of claim 8, wherein the capacitance is larger in a center pixel region centered among the plurality of pixel regions than in the other pixel regions.

10. The device of claim 8, wherein the pixel electrode is selected from a group consisting
15 of indium tin oxide (ITO) and indium zinc oxide (IZO).

11. The device of claim 8, wherein the common electrode is selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta), tungsten (W), antimony (Sb), and alloys thereof.

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12. The device of claim 8, wherein the common and pixel electrodes are on different layers.

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13. The device of claim 8, wherein the common electrode is electrically connected with the common line.

5 14. The device of claim 8, further comprising a first connecting line being electrically connected with the drain electrode.

15. The device of claim 14, wherein the first connecting line is electrically connected with the pixel electrode.

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